**HOMEWORK ASSIGNMENT Q No.2**

1. **Understanding the problem:**

In this question we have to design a 8:3 Encoder using case statement. 8:3 Encoder takes 8 bits as ip & gives three bit op.It is known as Octal to binary encoder. We will write cases of op for each value of ip.

**2)Devising a Plan**

In the ips we have A7 to A0 & for each row starting from 1st A0 to A7 takes value 1 & other values are zero.If A0=1 Op is binary 0 & so on.Hence we must take a 8 bit array as ip & take its various cases as the variable of case statement. According tovarious ip cases op will be executed.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **inputs** | | | | | | | | **outputs** | | |
| **A7** | **A6** | **A5** | **A4** | **A3** | **A2** | **A1** | **A0** | **Y2** | **Y1** | **Y0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

1. **Carrying out the plan:**

**Verilog code:**

module encoder(

input wire [7:0]a,

output reg [2:0]b

);

always@(a)

begin

case(a)

8'b00000001:b=3'b000;

8'b00000010:b=3'b001;

8'b00000100:b=3'b010;

8'b00001000:b=3'b011;

8'b00010000:b=3'b100;

8'b00100000:b=3'b101;

8'b01000000:b=3'b110;

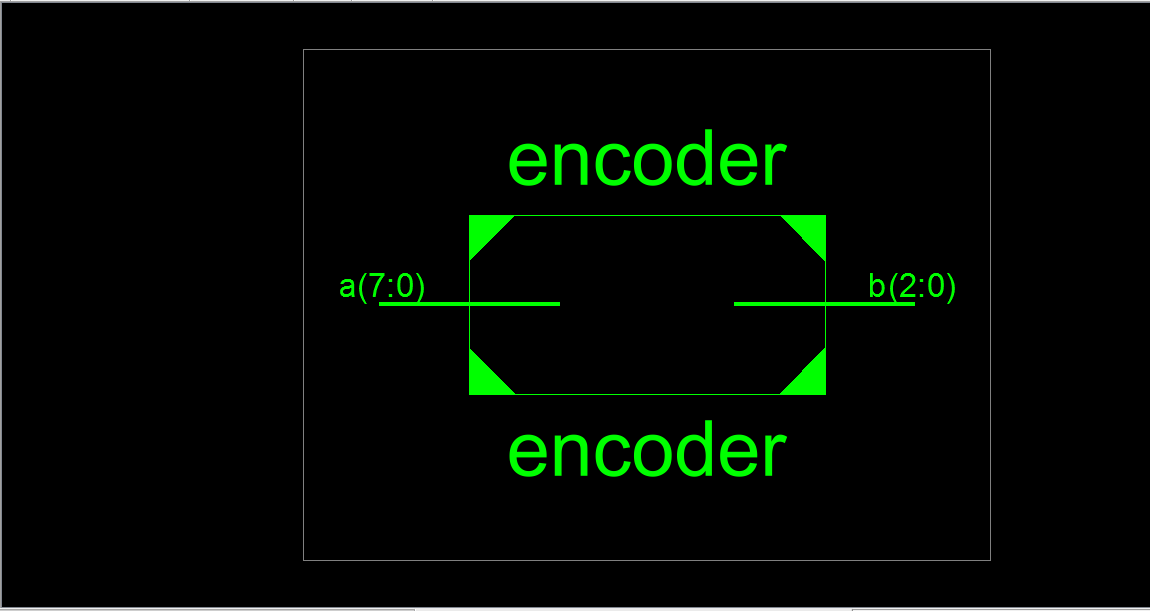
8'b10000000:b=3'b111;

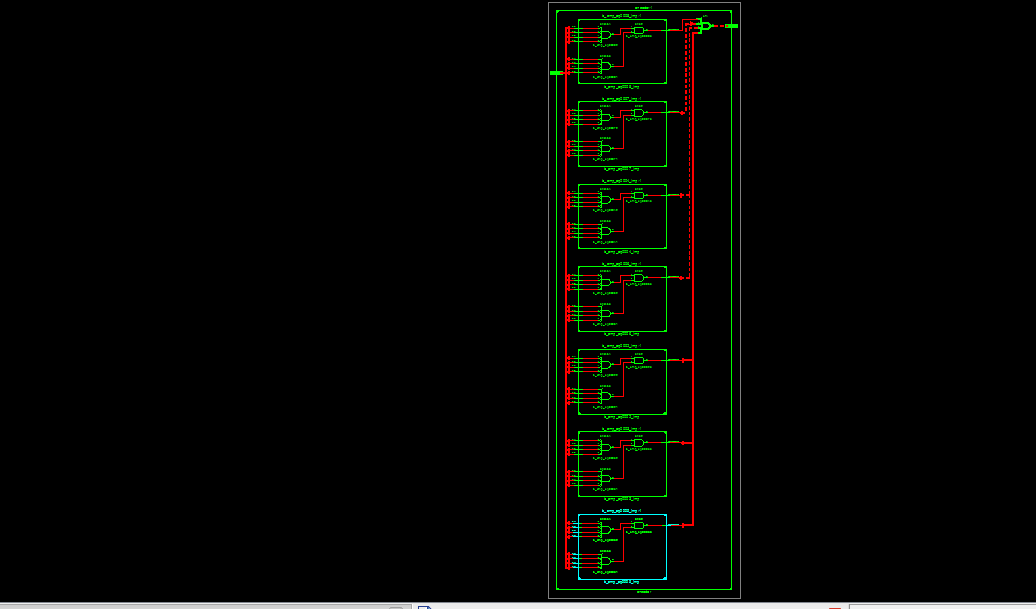
default:b=1'b0;

endcase

end

endmodule





**Testbench:**

module encoder\_tb;

// Inputs

reg [7:0] a;

// Outputs

wire [2:0] b;

// Instantiate the Unit Under Test (UUT)

encoder uut (

.a(a),

.b(b)

);

initial begin

// Initialize Inputs

a = 0;

// Wait 100 ns for global reset to finish

#100;

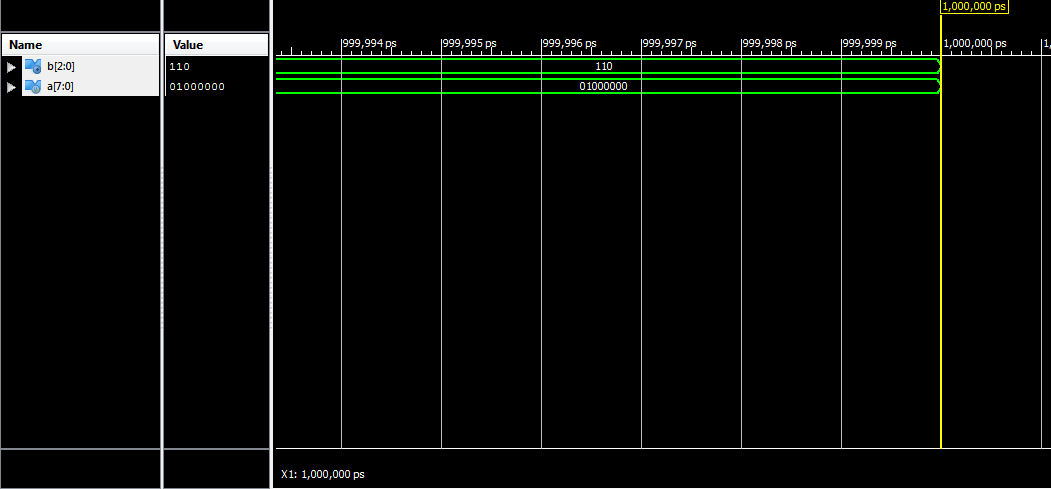
// Add stimulus here

a=8'b01000000;

#100;

end

endmodule



1. **Looking back/Self reflection**

In this program we executed 8:3 Encoder.We used case statements to design the encoder.This may even be done by ifelse loop.Encoder is used to code any code to machine code.here we are getting binary code at op.

***Synthesis report:***

Release 12.1 - xst M.53d (nt)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.52 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.52 secs

--> Reading design: encoder.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "encoder.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "encoder"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : encoder

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : encoder.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "encoder.v" in library work

Module <encoder> compiled

No errors in compilation

Analysis of file <"encoder.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <encoder> in library <work>.

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\* HDL Analysis \*

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Analyzing top module <encoder>.

Module <encoder> is correct for synthesis.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <encoder>.

Related source file is "encoder.v".

Unit <encoder> synthesized.

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HDL Synthesis Report

Found no macro

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Found no macro

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\* Low Level Synthesis \*

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Optimizing unit <encoder> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block encoder, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : encoder.ngr

Top Level Output File Name : encoder

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 11

Cell Usage :

# BELS : 9

# LUT2 : 3

# LUT4 : 6

# IO Buffers : 11

# IBUF : 8

# OBUF : 3

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 5 out of 1920 0%

Number of 4 input LUTs: 9 out of 3840 0%

Number of IOs: 11

Number of bonded IOBs: 11 out of 141 7%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.305ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 24 / 3

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Delay: 9.305ns (Levels of Logic = 4)

Source: a<6> (PAD)

Destination: b<2> (PAD)

Data Path: a<6> to b<2>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 3 0.715 1.066 a\_6\_IBUF (a\_6\_IBUF)

LUT4:I0->O 1 0.479 0.976 b<2>62 (b<2>62)

LUT2:I0->O 1 0.479 0.681 b<2>76 (b\_2\_OBUF)

OBUF:I->O 4.909 b\_2\_OBUF (b<2>)

----------------------------------------

Total 9.305ns (6.582ns logic, 2.723ns route)

(70.7% logic, 29.3% route)

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 6.16 secs

-->

Total memory usage is 185720 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)